ARF26
User Guide

GENERAL USE

The ARF26 radio module is a multi-channel FSK digital transmission radio-frequency transceiver using the 868-870 MHz band. This transceiver proposes up to 9 transmission channels enabling two-way half-duplex digital links up to 25 kBps Manchester. The transceiver is composed of "rough" radio components; the transmission protocol (data encoding/decoding) and radio module programming are performed by the associated logic.

CHOICE OF TRANSMISSION CHANNELS

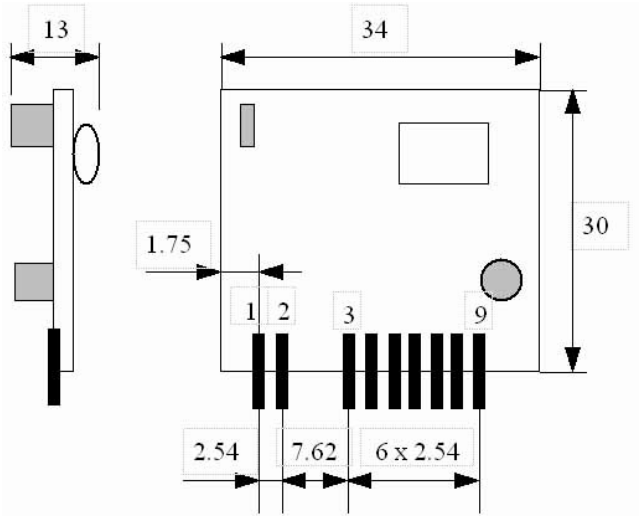
The 868-870 MHz band is subdivided into 4 sub-bands authorising different duty cycles: ≤ 0.1 %, ≤ 1%, ≤ 10% and ≤ 100%. The duty cycle of the product has to be calculated to know which of the sub-bands can be used by the application. The table below presents the different sub-bands with their duty cycle and the maximum number of channels that can be envisaged in each sub-band.

Sub-band n°	1	2	3	4
Band edges (in MHz)	868-868.6	868.7-869.2	869.4-869.65	869.7-870 (*)
Duty cycle	≤ 1%	≤ 0.1 %	≤ 10%	up to 100%
Maximum number of channels	3	3	1	2

(*) The maximum apparent radiated power for sub-band #4 is limited to +7dBm.
The table below gives the details of the available channels:

Sub-band	Channel	Frequency
868-868.6 MHz duty cycle 1%	1	868.100 MHz
	2	868.300 MHz
	3	868.500 MHz
868.7-869.2 MHz duty cycle 0.1%	4	868.783 MHz
	5	868.950 MHz
	6	869.117 MHz
869.4-869.65 MHz duty cycle 10%	7	869.525 MHz
869.7-870 MHz duty cycle 100%	8	869.775 MHz
	9	869.925 MHz

DIMENSIONS / PIN ASSIGNMENTS



1 - GND RF
2 - ANTENNA
3 - VDC: 3 to 5V power supply
4 - GND: 0V ground
5 - DATAMSG: Data input/output
6 - SLE: Enable input
7 - SCK: Clock input
8 - SDATA: Programming data input/output
9 - DATACLK: Received data synchronisation clock

N.B.:
- The signals SLE, SCK and SDATA correspond to the 3-wire serial interface for programming the transceiver registers.
- The radio module is supplied by an external power source between VDC and GND. The supply voltage should be chosen in the 3-5V range.

CHANNEL MANAGEMENT

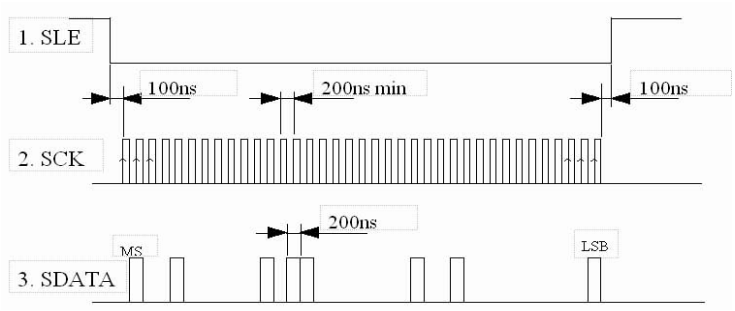
- **Principle**

The transmitter and receiver have to be configured (frequency registers, control registers...) to establish the radio link. This register configuration is performed by means of the SLE, SCK and SDATA 3-wire serial bus.
The number of registers to be programmed depends on the operating mode: transmission, receipt... Each word is programmed starting with the most significant bit (MSB) and each bit is loaded on the rising front of SCK.

N.B:
- In transmission mode (Tx) and receipt mode (Rx), the programming is different for any one channel.
- The transmitter and receiver have to work on the same channel to “understand” each other.
- For this programming, it is understood that low level corresponds to GND and high level to VDC.

- **Timings**

Programming of a register is performed according to the following timing diagram:



N.B.:
- The number of pulses for SCK corresponds to the number of bits to be sent and depends on the register. In the example above, there are 37 clock pulses that correspond to the longest register.
- Between programming of 2 registers, SLE must be kept at "1" for a minimum time of 200 ns.
- The content of the registers (address included) for each operating mode is specified in the following paragraphs. When programming a register, it is imperative to send the specified number of bits (cf. tables below), no more no less, to avoid an incorrect programming.

- **Transmission mode**

In transmission mode, three 37-bit registers (the control register CTRL1 and frequency registers F0 and F1) and one 7-bit register (control register CTRL3) have to be configured. Programming of the registers must begin with F0, followed by F1, then CTRL3 and finish with CTRL1. The table below presents the content of the registers according to the channel:

Channel	F0 (hex) **37 bits**	F1 (hex) **37 bits**	CTRL3 (hex) **7 bits**	CTRL1 (hex) **37 bits**
1	019CD440E2	03085464E6	45	09DB005260
2	01A57D72C4	034465D4C4		
3	01FD05E6DE	03449DC4FA		
4	01019DF274	0380CDF472		
5	0188C45666	03855552F4		
6	018804F4EE	03B195D248		
7	01405DE244	03518540C4		
8	01059DC6F4	03A1154240		09DB002260
9	01FC3DE658	03506D467E		

- **Receipt mode**

In receipt mode, at least two 37-bit registers (the control register CTRL1 and frequency register F2) and one 7-bit register (CTRL3) have to be configured. Programming of the registers must start with F2, followed by CTRL3 and finish with CTRL1. The table below presents the content of the registers according to the channel:

Channel	F2 (hex) **37 bits**	CTRL3 (hex) **7 bits**	CTRL1 (hex) **37 bits**
1	05C14DD4C8	44	0990000260
2	05B57DD2C4		
3	05597C52E2		
4	058884E26E		
5	0539E5D4D0		
6	05C91C50EA		
7	056DFD46D8		
8	052D6544D0		
9	05783DE2D8		

- **"DATACLK" mode**

In receipt mode, a received data synchronisation clock can be available on the DATACLK pin of the radio module (rising front in the middle of the data). To take advantage of this option, the control register CTRL2 (27 bits) also has to be configured according to the maximum transmission rate of the application. In "DATACLK" mode, programming must be started with F2, followed by CTRL2 then CTRL3, and finally CTRL1.
The table below presents the content of CTRL2 according to the maximum transmission rate of the application and the content of CTRL1 that has changed (for activation of the DATACLK).

Transmission rate	Transmission rate (in Manchester)	CTRL2 (hex) **27 bits**	CTRL1 (hex) **37 bits**
2 kBps	1 kBps	7D40266	09B0000260
2.4 kBps	1.2 kBps	7D0AD55	
4kBps	2 kBps	7CA0133	
4.8kBps	2.4 kBps	7C8562B	
9.6 kBps	4.8 kBps	7C42B15	
10 kBps	5 kBps	7C40014	
19.2 kBps	9.6 kBps	7C2160B	
20 kBps	10 kBps	7C2000A	
39.2kBps	19.6 kBps	7C10C05	
40 kBps	20 kBps	7C10005	
50 kBps	25 kBps	7C0CD04	

N.B.:
- The content of CTRL1 is identical whatever the channel.
- In “DATACLK” mode, the contents of the registers F2 and CTRL3 are the same as in paragraph 5.4.
- Consult us for other transmission rates.

- **Standby mode**

To switch to Standby mode, the registers CTRL3 then CTRL1 have to be programmed:

CTRL3 (hex) **7 bits**	CTRL1 (hex) **6 bits**
45 (*)	12

(*): When switching to Standby mode from transmission mode, the register CTRL3 is already at 45 (hex).

To return to the previous mode, CTRL1 and possibly CTRL3 have to be reprogrammed:

Previous mode	CTRL3 (hex) **7 bits**	CTRL1 (hex) **6 bits**
Transmission	-	13
Receipt	44	13

- **Reset**

Reset of all the registers is performed by programming the RESET register:

	RESET (hex) **6 bits**
Content:	2E

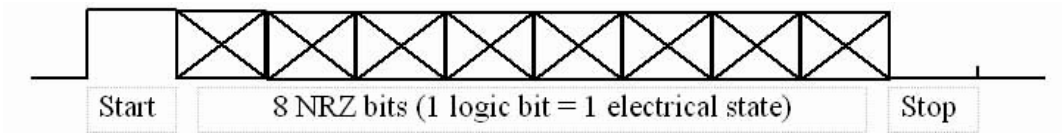
After a reset, the radio module is in standby mode and all the registers have to be reprogrammed as described above to switch to transmission or receipt mode.

PROTOCOL

On account of the ARF26 system transmission principle and of the modulation in phase lock loop, the modulating signals must have a **frequency comprised between 1 kHz and 25kHz**. Lower and higher frequencies cannot be transmitted, as they are filtered. This means, among other things, that the link cannot transmit constant states with a duration of more than 500 µs.

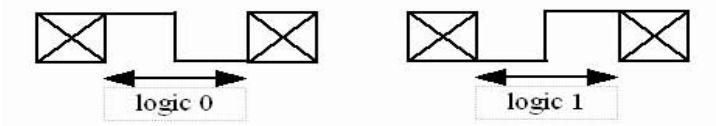
- **Level - Bit Encoding**

Most conventional hardwired serial links transmit bytes in asynchronous manner using an NRZ type encoding (1 logic bit = 1 electrical state). This results in the spectrum occupation of the signals thus generated being about one decade. Furthermore, sampling of the bytes thus received supposes perfect synchronisation of decoding on the start bit.

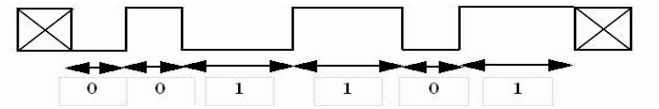


In the case of radio transmission, it is preferable to limit the spectrum of the signals to be transmitted as far as possible, in particular towards low frequencies, even if this means increasing the main frequency. Moreover, it is advantageous to reset the synchro on each transmitted bit; receivers are in fact the cause of large duty cycle errors on the electrical states. Bit encodings should therefore be preferred, for example those proposed below:

Manchester or two-phase:

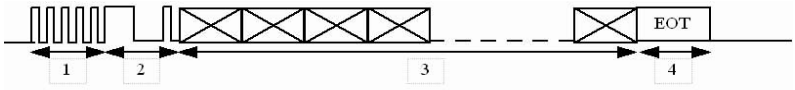


Differential PWM:



- **Level - Frame Encoding**

Once the bits have been encoded, it is then imperative that they be transmitted according to a frame structure; the radio link is very sensitive to binary flow breaks which can only be minimised by “serialising” the bytes.
A conventional frame structure is shown below:

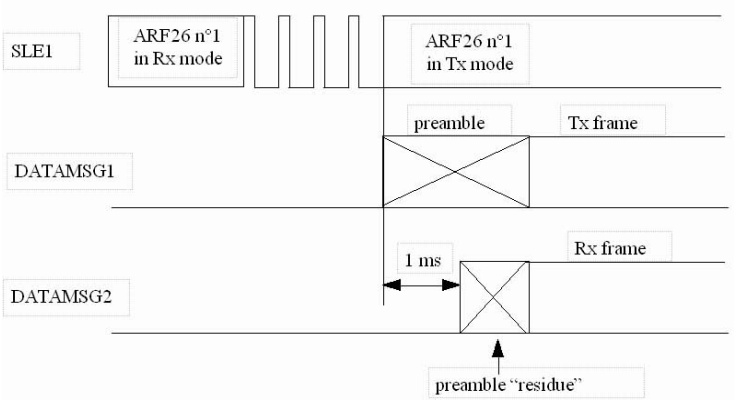


1 **Preamble**: Electrical succession 101010... to fix the receiver polarisation and compensate the channel settling time.
2 **Start pattern**: Electrical pattern that marks the beginning of the useful data by a break in the binary flow of the preamble.
3 **Useful part**: Successions of bytes encoded at bit level.
4 **Stop pattern**: Indicates the end of frame (necessary when the frame may be of variable length).

RADIO CHANNEL MANAGEMENT

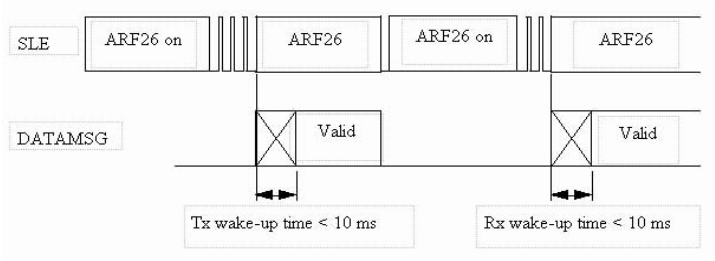
- **Radio channel setting:**

This characteristic corresponds to the time required for the first valid bits to be obtained on receipt on an ARF26 n°2 (DATAMSG2) after a frame has been transmitted from another distant ARF26 n°1 module (DATAMSG1).



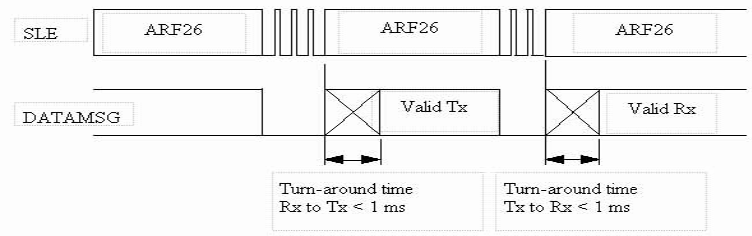
- **Wake-up time (Start-up time):**

This characteristic corresponds to the time required to switch from Standby mode (low consumption) to 'active' mode (transmission or receipt).



- **Transceiver turn-around:**

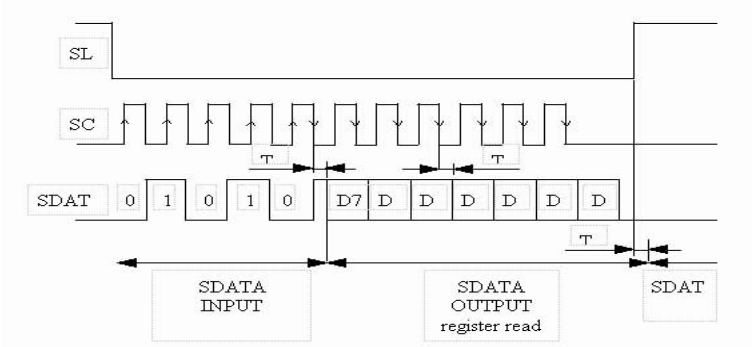
This characteristic corresponds to the time required to switch from transmission to valid receipt or vice-versa on the same device, and therefore to a TX_RX control input status change.



RSSI

The 3-wire serial bus is bi-directional. It is therefore possible to read the status of certain registers. The value of the RSSI (received signal strength indicator) is contained in the status register in the form of a 6-bit word.
To know the value of these 6 bits, you have to go and read the status register according to the following timing diagram:

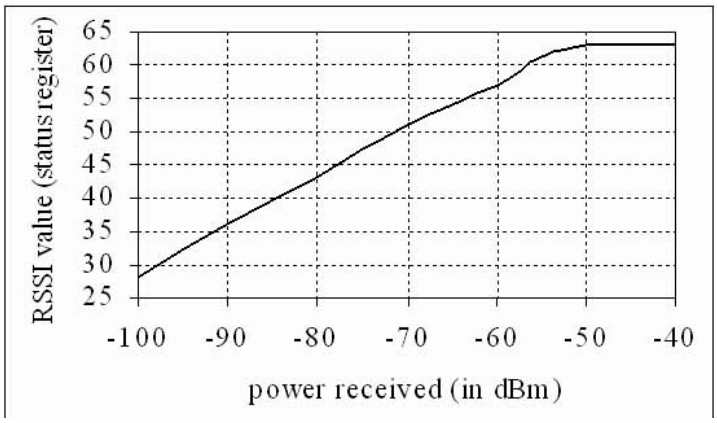
- The first 4 bits (0101) correspond to the status register address.
- The 5th bit (1) selects register read mode.



T1: SDATA switching time from input to output on descending front of SCK: 50 ns max.
T2: data propagation delay time after a descending front: 50 ns max.
T3: SDATA switching time from output to input on rising front of SLE: 50 ns max.

The timings indicated in chapter 4.2 remain valid.

The value of the RSSI corresponds to bits D1 (LSB) to D6 (MSB). Bit D7 is of no interest.
The graph below gives a correspondence between the RSSI value and the received power level.



Caution:

- The RSSI level remains an indicator which has to be used with precaution. The curve presented above may change somewhat from one product to the other.

- This RSSI level can also indicate the presence of a possible interfering source on the channel used. It is not possible to ensure that the required signal coming from the remote transmitter is detected and received by examining the RSSI only. The identity of the transmitter also has to be checked by encodings in the transmitted frames.

The RSSI is a necessary but non-sufficient condition for obtaining correct receipt.

SPECIFICATIONS

		3V	5V
TRANSMITTER			
Frequencies	868-870 MHz 9 channels		
Power developed (/ 50 Ohms)		8 dBm (*)	10 dBm (*)
Modulation	2FSK +/-25 kHz		
Consumption		55 mA	60 mA
RECEIVER			
Technology	Super-heterodyne with double frequency change		
Frequencies	868-870 MHz 9 channels		
Sensitivity (at S/N 15dB)	2.2 µV (-100 dBm)		
Demodulation	2FSK +/-25 kHz		
Bandwith	2 MHz front end 100 kHz back end		
Digital output	0/Vdc		
Consumption		32 mA	40 mA
COMPLETE SYSTEM			
Operating voltage	from 3 to 5V (+/- 5%)		
Standby current		< 2µA	<2 µA
Transmission rate	from 1 to 25 kbps Manchester		
Transmitter wake-up time	10 ms		
Receiver wake-up time	10 ms		
Turn-around time Tx to Rx	1 ms		
Turn-around time Rx to Tx	1 ms		
Channel setlling time	1 ms		
Temperature	-20°C to +70°C		

INTEGRATION

- **Daughter board:**

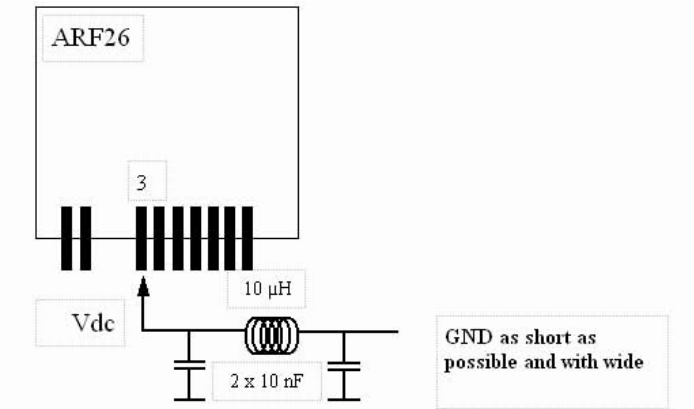
This daughter board is to be incorporated directly on an electronics mother board by means of the "COMCLIP" connectors provided on the radio module (cf. dimensions and pin assignment in chapter 3 of this document).

The mother board can be used to locate the antenna output by means of a 50 Ω printed line. This line is formed by a printed track 2.5 mm wide which must be situated above a continuous ground plane (the HF cold point is to be connected as short as possible to this plane). Avoid running close to digital lines!

- **EMC aspect:**

When a radio element is integrated in an electronics system, the mother board must be provided with a ground plane which is as continuous as possible. The GND and GND RF signals of the module are to be connected as short as possible to this plane. It is preferable that the module then be fitted on the ground plane side, opposite from the tracks.

Due to the presence of a Receiver part (for the transceiver), some precautions have to be taken when integrating the ARF26 module. Fitting a receiver with a good sensitivity alongside a high-speed digital part requires a little succinct filtering described by the diagram below:



A RECEIVER WITHOUT A SQUELCH GENERATES NOISE ON OUTPUT IN THE ABSENCE OF A RECEIPT SIGNAL. THIS DOES NOT HOWEVER MEAN THAT IT IS POLLUTED BY INTERFERENCE; THE DATA WILL BE "CLEAR" WHEN RECEIPT TAKES PLACE.

REGULATION COMPLIANCE

When using radio transceivers in the form of integrated daughter boards, conformity with regulation compliance relates to the finished product.
In Europe, finished products must comply with the RTTE directive. For this type of radio application, conformity with the RTTE directive will be established by compliance with the following requirements:

- EN300220 standard (Efficient use of Radio/ spectrum).
- EN301489 standard (EMC).
- EN60950 standard (Electrical safety if necessary)

Important:

Although the ARF26 daughter boards comply with the criteria and dimensions of the EN300220 radio standard, their integration in a "mother" electronic system may modify some electrical characteristics (harmonic levels, spurious RF, etc.)
Before it is sent for laboratory tests, the product therefore has to be examined on our premises to check that it complies with regulations. After presentation, the product and the test reports must be kept as proof of conformity.